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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,044	12/04/2001	Gilbert C. Sih	010264	9617

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Qualcomm Incorporated
Patents Department
5775 Morehouse Drive
San Diego, CA 92121-1714

EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/006,044	SIH ET AL.	
	Examiner	Art Unit	
	Hau H. Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) *6,21,22,27 and 36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-5,7-20,23-26,28-35,37 and 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Arguments

1. Applicant's arguments with respect to claims 1-38 have been considered but are moot in view of the new grounds of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 23-26, and 28, recite the limitations "the device of claim 21" and "the device of claim 22". There is insufficient antecedent basis for this limitation in the claim because claims 21 and 22 have been canceled.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by McGuiness (U.S. Patent No. 6,104,416).

Referring to claims 1-3, McGuiness teaches a video decoder 160 that uses motion compensated prediction in decompressing frames as shown in Fig. 3, comprising a DMA engine 178 (a VDMA)that controls all of the interfaces with DRAM picture memory 180 (col. 5, lines 28-29), the memory 180 is linearly addressable memory (col.8, lines 9-12). With reference to Fig. 7, McGuiness teaches retrieving the digital array 400 for display. All of the pixels in the

first row 406 of the first tile 402 are read by reading the first word 408 of the memory 410. Since there are 16 bytes in a row of a tile the line increment for the read is 16. The pixels in the first row 416 of the next tile are read by reading the word 417 at the word address of the first word 408 plus X (a jump parameter indicating the number of storage units). Because the two words 408 and 416 are only 64 words apart, they can both be accessed during the same burst of a page mode access of the memory. This process is continued until all the words containing data in the row 401 are read. The pixels are sent to a buffer and then to a display. After the entire row 401 is sent to the display the next row 403 is read and sent to the display (fetching multidimensional block of video data from non-contiguous rows of the memory). FIG. 9 shows how an arbitrary rectangular array portion 252 of the picture 250 is retrieved from the memory (col. 12, lines 32-62), and a command for accessing the memory specifies a number of rows and a number of columns for the block of video data as disclosed on column 12, lines 63-67.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 4-5, 7-20, 23-26, 28-35, 37, and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over McGuiness (U.S. Patent No. 6,104,416) in view of Kohn (U.S. Patent No. 6,335,950).

Referring to claims 4, 7-8, as cited above, McGuiness teaches all the limitations of claims 4, 7-8, including a motion estimation unit, except that: the VDMA controller copies the video data from the memory to a destination memory; the system further comprising a processor issuing command to the VDMA via a first bus, and a digital signal processor issue commands to the VDMA via a second bus; and the system further comprising a motion estimation unit having a differential calculator.

However, as shown in Fig. 1, Kohn teaches a system for processing and encoding video data comprising a processor 102, a video DSP 104, and a motion estimation engine 100, and further teaches the video DSP 104 works in parallel with the processor 102 to off-load compute intensive pixel level processing operations. Internally, the video DSP 104 contains a separate DMA processor (a video DMA) and a DSP processor connected by a double buffered working memory. The DMA processor transfers data to and from the external SDRAM 200 while the DSP processor performs signal processing operation (which implied that the DMA processor communicates with the DSP processor via a bus (second bus) different from the first bus (bus 103 and 105), which communicates between the DSP processor and the processor 102 (col. 4, lines 3-20). Fig. 2 shows the details of the motion estimation 100, which comprises an internal cache 212-215 (destination memory) for coping video data from external memory 200 (source memory), a differential calculator 216 for calculating distortion metrics between blocks of video data (see also to Fig. 4, and col. 5, lines 49-56).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kohn in combination with the method of storing and retrieving video data from memory as taught by McGuiness in order to off-loads much of the motion estimation processing

from the processor while allowing the processor to retain full control of critical search parameters, thus, flexibility and high performance are maintained (col. 3, lines 1-8).

In regard to claim 5, McGuiness teaches specifying a starting address of the video block to be retrieved as shown in Fig. 9. Although McGuiness does not teach specifying a starting address in the destination memory, Kohn teaches transferring block of video data from a source memory to a destination memory. Thus, it is implied that the destination memory is also specified with a starting address.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kohn in combination with the method of storing and retrieving video data from memory as taught by McGuiness in order to off-loads much of the motion estimation processing from the processor while allowing the processor to retain full control of critical search parameters, thus, flexibility and high performance are maintained (col. 3, lines 1-8).

Referring to claims 9-16, 31-35, 37-38, as cited above, McGuiness teaches a method of retrieving a block of video data from a linearly addressable memory in response to a DMA command, including generating a set of addresses corresponding to multiple non-contiguous rows of a source memory, and the addresses generated including specifying a number of rows and columns, and also teach specifying a jump parameter indicating the number of addresses between each row of the video block. McGuiness also teaches a motion estimation unit having an internal memory. Thus, McGuiness et al. teach all the limitations of claims 9-16, 31-35, 37-38, except for copying a video data from a source memory to a destination memory according a source addresses and destination addresses, and except for receiving the command via a first bus, and receiving a second command via a second bus.

Kohn, as cited above, teaches a method of transferring block of video data from a source memory to a destination memory, and further teach the DMA command received from a processor via a first bus, and the DSP command to the DMA controller is received via a second bus.

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kohn in combination with the method of storing and retrieving video data from memory as taught by McGuiness in order to off-loads much of the motion estimation processing from the processor while allowing the processor to retain full control of critical search parameters, thus, flexibility and high performance are maintained (col. 3, lines 1-8).

Referring to claims 17-20, 23-26, 28-30, as cited above, McGuiness teaches a method of retrieving a block of video data from a linearly addressable memory in response to a DMA command, including generating a set of addresses corresponding to multiple non-contiguous rows of a source memory, and the addresses generated including specifying a number of rows and columns, and also teach specifying a jump parameter indicating the number of addresses between each row of the video block. McGuiness also teaches a motion estimation unit having an internal memory. Thus, McGuiness et al. teach all the limitations of claims 17-20, 23-26, 28-30, except for: copying a video data from a source memory to a destination memory according a source addresses and destination addresses; receiving the command via a first bus, and receiving a second command via a second bus; and a command buffer to store search commands.

Kohn, as cited above, teaches a method of transferring block of video data from a source memory (200, Fig. 1) to a destination memory, which includes a first memory (212, 213) and a second memory (214, 215) (Fig. 2), and further teach the DMA command received from a

processor via a first bus, and the DSP command to the DMA controller is received via a second bus. As shown in Fig. 2, Kohn further teaches the motion estimation unit 100 comprises a command memory 204 for storing search commands and delivering the commands to the differential calculator 216 (col. 4, lines 61-67, and col. 5, lines 1-10), and the differential calculator perform reading video block from the first memory (212, 213) and the second memory (214, 215) in parallel (col. 5, lines 39-53).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Kohn in combination with the method of storing and retrieving video data from memory as taught by McGuiness in order to off-loads much of the motion estimation processing from the processor while allowing the processor to retain full control of critical search parameters, thus, flexibility and high performance are maintained (col. 3, lines 1-8).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 571-272-7787. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 571-272-7778.

The fax number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system contact the Electronic Business Center (EBC) at 866-2 17-9197 (toll-free).

H. Nguyen

8/17/2005

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600